REMARKS

Claims 34-37, 46 and 53-61 are pending in the present application. Claims 34, 46, 53, 54, 57 and 59-61 have been amended.

Claim Rejections-35 U.S.C. 103

Claims 34, 37, 46, 53, and 57-61 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Egawa reference (U.S. Patent No. 6,229,215) in view of the Buckley, III et al. reference (U.S. Patent No. 5,477,082). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 34 includes in combination among other features a BGA (ball grid array) type semiconductor device "including a base plate, a first semiconductor element mounted on the frontside surface of the base plate, a first resin that seals an upper surface of the semiconductor element and the frontside surface of the base plate, and a plurality of bumps formed on a backside surface of the base plate that is opposite the frontside surface"; a CSP (chip size packaged) type semiconductor device "mounted on an area of the backside surface of the base plate of said BGA type semiconductor device which does not have the plurality of bumps formed thereon,...wherein the back surface and the entirety of the side surfaces of the second semiconductor element are exposed". As further featured, the CSP type semiconductor device "has a second resin that covers the main surface of the second semiconductor element and side surfaces of the terminals, the first and second resins

are separate from each other". Applicants respectfully submit that the semiconductor device of claim 34 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

The Examiner has primarily relied upon Figs. 2 and 4 of the Egawa reference as taken together. However, Fig. 2 of the Egawa reference is a cross section of a semiconductor device of a **second embodiment**, while in contrast Fig. 4 of the Egawa reference illustrates a method for manufacturing a semiconductor device of a **third embodiment**. Accordingly, in formulating this rejection, the Examiner has relied upon separate and distinct second and third embodiments of the Egawa reference.

That is, in the Fig. 2 embodiment of the Egawa reference, semiconductor chip 17 (presumably interpreted by the Examiner as the second semiconductor element of claim 34) has side surfaces thereof which are covered by resin. Accordingly, the structure in the Fig. 2 embodiment of the Egawa reference modified to be mounted on a printed circuit board in view of the Buckley, III et al. reference as suggested by the Examiner, would not include a CSP type semiconductor device having a second semiconductor element wherein a back surface and the entirety of side surfaces of the second semiconductor element are exposed, as would be necessary to meet the features of claim 34.

On the other hand, although semiconductor chip 17 as shown in the Fig. 4 third embodiment of the Egawa reference has a back surface and side surfaces which are exposed, the structure as shown in connection with the processing step described with

respect to Fig. 4 of the Egawa reference includes base plate 30 having through-hole 31 therein. Injected resin 33 reaches the surface of the second semiconductor chip 17 by way of through-hole 31, **in a single injection process**. That is, the same resin seals both the front side surface of base plate 30 and the main surface of second semiconductor chip 17. The Fig. 4 third embodiment of the Egawa reference thus does not disclose first and second resins that are separate from each other, as would be necessary to meet the features of claim 34.

Moreover, in both of the second and third embodiments as shown with respect to Figs. 2 and 4 of the Egawa reference, semiconductor chip 11 (presumably interpreted as the first semiconductor element of claim 34) does not have a resin that seals an upper surface thereof, as would be necessary to meet the still further features of claim 34.

In the cover figure (Fig. 3) of the secondarily relied upon Buckley, III et al. reference, a PC card 52 is disclosed with flexible carrier 60 mounted thereon via solder ball array 54. As described in column 3, lines 46-47 of the Buckley, III et al. reference, an encapsulant such as epoxy (not shown) is placed around die 56 and 58 to provide mechanical strength and reliability. However, since heat sink 64 is shown as attached to die 56 (presumably interpreted as corresponding to the first semiconductor element of claim 34), the Buckley, III et al. reference does not disclose a first resin that seals an upper surface of a first semiconductor element, and that is separate from a second resin, as would be necessary to meet the features of claim 34. Modification of the Fig.

3 structure of the Buckley, III et al. reference to include a sealing resin intermediate the upper surface of die 56 and heat sink 64 would appreciably reduce heat transfer between die 56 and heat sink 64, defeating the purpose of the structure.

The Buckley, III et al. reference thus would provide no motivation to modify the second or third embodiments of the primarily relied upon Egawa reference to meet the features of claim 34. Applicants therefore respectfully submit that the semiconductor device of claim 34 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 34, 37, 46 and 57-59, is improper for at least these reasons.

The semiconductor device of claim 53 includes in combination among other features a BGA (ball grid array) type semiconductor device "including a base plate, a first semiconductor element mounted on a frontside surface of the base plate, a first resin that seals an upper surface of the first semiconductor element and the frontside surface of the base plate, and a plurality of bumps formed on a backside surface of the base plate that is opposite the frontside surface"; and a CSP (chip size packaged) type semiconductor device "mounted on an area of the backside surface of the base plate of said BGA type semiconductor device which does not have the plurality of bumps formed thereon,...wherein the back surface and the entirety of the side surfaces of the second semiconductor element are exposed,... the first and second resins are separate from each other".

Applicants respectfully submit that the prior art as relied upon by the Examiner

taken singularly or together does not disclose separate first and second resins, whereby the first resin seals an upper surface of a first semiconductor element, and whereby a back surface and the entirety of side surfaces of the second semiconductor element are exposed, as would be necessary to meet the features of claim 53. In the Fig. 2 second embodiment of the Egawa reference, semiconductor chip 17 (presumably interpreted as the second semiconductor element of the claims) does not have side surfaces that are exposed from resin. Moreover, in the Fig. 4 third embodiment of the Egawa reference, a single injected resin is used, whereby first and second resins separate from each other are not disclosed. Also, the upper surface of semiconductor chip 11 in both the Fig. 2 second embodiment and the Fig. 4 third embodiment of the Egawa reference are not sealed with a first resin.

The secondarily relied upon Buckley, III et al. reference does not overcome the above noted deficiencies of the Egawa reference, at least because die 56 (presumably interpreted as corresponding to the first semiconductor element) in the cover figure has heat sink 64 disposed directly on the upper surface of die 56. That is, the upper surface of die 56 is not sealed by a first resin that is separate from a second resin, as would be necessary to meet the features of claim 53. Applicants respectfully submit that the semiconductor device of claim 53 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 53, 60 and 61, is improper for at least these reasons.

Claims 35, 36 and 54-56 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Egawa and Buckley, III et al. references, in further view of the Lin et al. reference (U.S. Patent No. 5,239,198). As emphasized previously in the Amendment dated October 21, 2008, passive electronic component 50 as shown in Figs. 6 and 7 of the Lin et al. reference is not specifically described as a CSP (chip size packaged) type semiconductor device. Moreover, passive electronic component 50 is not specifically described or shown as having a main surface sealed with a second resin, wherein portions of each of a plurality of terminals are exposed from the second resin. Accordingly, Applicants respectfully submit that claims 35, 36 and 54-56 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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